REMARKS

This communication is a full and timely response to the aforementioned Office Action dated October 21, 2010. Claims 1, 2 and 5-22 are not amended and remain in the application. Thus, claims 1, 2 and 5-22 are pending in the application. Claims 1 and 14-17 are independent.

Reconsideration of the application and withdrawal of the rejections of the claims are respectfully requested in view of the following remarks.

I. Rejections Under 35 U.S.C. § 103

A. Claims 1, 12-18 and 21-22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Inaba et al. (U.S. Patent No. 5,477,557, hereinafter "Inaba") in view of Kobayashi et al. (U.S. Patent No. 6,181,718, hereinafter "Kobayashi") and Nagarajan et al. (U.S. Patent No. 5,760,939, hereinafter "Nagarajan").

This rejection is respectfully traversed. With the claimed invention as a road map, the Office applied bits and pieces of the above-described references in an attempt to arrive at the claimed invention. However, the Office's proposed modification is derived from Applicants' disclosure. Applicants respectfully submit that it would not have been obvious to modify the references in the manner proposed by the Office to arrive at the features of the claimed invention. The applied references, either individually or in combination, do not disclose, suggest or contemplate the combination of features recited in claims 1 and 14-17, as well as the claims depending therefrom.

In the final Office Action dated March 12, 2010, independent claims 1 and 14-17 were rejected on the basis of Inaba and Kobayashi references. In the Amendment filed on September 9, 2010, claims 1 and 14-17 were each amended to recite the features of cancelled dependent claim 4. For example, with reference to the embodiment of Figure 1 of the present application, claims 1 and 14-17 were each amended to recite the arrangement of a resistor 22b connected in parallel with an inductance element 21b to the anode of an optical semiconductor element (e.g., laser diode) 20.

In the aforementioned final Office Action, the Office acknowledged that Inaba and Kobayashi do not disclose the features of claim 4. In the September 9, 2010

Amendment, it was demonstrated that Nagarajan does not disclose the arrangement of a resistor connected in parallel with an inductance element to an anode of an optical semiconductor element. On the contrary, with reference to Figure 1, Nagarajan discloses a DC bias circuit 16 in which an inductor and resistor are connected in parallel to the cathode of diode 14.

In the present Office Action, the Office tacitly acknowledged the deficiencies of the applied references and modified its interpretation and application of the references in an attempt to arrive at the claimed invention, with the claimed invention as a road map. For instance, the Office now alleges that although Nagarajan does not disclose the arrangement of a resistor connected in parallel with an inductance element to an anode of an optical semiconductor element, it would have been obvious to do so based on the combination of Inaba, Kobayashi and Nagarajan references (see "Response to Arguments" section on pages 2 and 3 of the Office Action). Applicants respectfully submit that this assertion is not supportable.

With reference to Figure 1, for example, an exemplary embodiment of the present disclosure provides an optical semiconductor device that includes an optical semiconductor element (e.g., laser diode (LD) 20) having a cathode and an anode. The optical semiconductor device also includes a first conductor line (e.g., lower line extending from the distributed constant circuit 18) connected to the cathode of the optical semiconductor element, and supplying a first electric signal (e.g., positive phase signal) to the optical semiconductor element (e.g., LD 20). The optical semiconductor device also includes a second conductor line (e.g., lower line extending from the distributed constant circuit 18) connected to the anode of the optical semiconductor element (e.g., LD 20), and supplying a second electric signal (e.g., anti-phase signal) to the optical semiconductor element (e.g., LD 20).

As described beginning at line 2 on page 20 of the original specification, and as illustrated in Figure 1, the optical semiconductor device of the exemplary embodiment also includes a first inductance element (e.g., solenoid 21a) connected to the cathode of the optical semiconductor element (e.g., LD 20) and the first conductor line. In addition, the exemplary optical semiconductor device includes a second inductance element (e.g., solenoid 21b) connected between the anode of the optical semiconductor element (e.g., LD 20) and a ground potential (e.g., the ground

potential above the upper horizontal dotted line denoting LD module 2) such that one end of the second inductance element (e.g., solenoid 21b) is connected at the ground potential. The disclosed embodiment provides that the second inductance element (e.g., solenoid 21b) is also connected to the second conductor line.

The optical semiconductor device of the exemplary embodiment also includes a first bias circuit (e.g., bias circuit 28a), which includes the first inductance element (e.g., solenoid 21a) and a first resistor (e.g., resistor 22a) connected in parallel to the first inductance element (e.g., solenoid 21a). In addition, the optical semiconductor device of the exemplary embodiment includes a second bias circuit (e.g., bias circuit 28b), which includes the second inductance element (e.g., solenoid 21b) and a second resistor (e.g., resister 22b) connected in parallel to the second inductance element (e.g., solenoid 21b). As described in lines 8-10 on page 21 of the specification, for example, the first and second bias circuits act as ungrounded open terminals for high frequencies.

Independent claims 1 and 14-17 recite various features of the above-described features of the exemplary embodiments described above. For conciseness, the Office's rejection of claim 1 is mainly discussed below. Independent claims 14-17 recite similar features to those of claim 1. Applicants respectfully submit that the applied references do not disclose, suggest or contemplate all the recited features of the claimed invention.

With reference to Fig. 2 of Inaba, the Office alleges that the line between the collector of transistor Q2 and the anode of diode LD corresponds to the second conductor line as recited in claim 1. The Office also alleges that the line between the cathode of diode LD and the collector of transistor Q1 of Inaba corresponds to the first conductor line as recited in claim 1. The Office alleges that the inductor connected to the cathode of diode LD and the collector of transistor Q4 of Inaba corresponds to the first inductance element as recited in claim 1.

However, the Office concedes that Inaba does not disclose, suggest or contemplate the arrangement of the second inductance element as recited in claim 1. For instance, the Office acknowledges that Inaba does not disclose an inductor connected between the anode of diode LD and the ground potential, which is below

the node between the collector of transistor Q2 and the anode of diode LD. In an attempt to arrive at this feature, the Office applied Kobayashi.

In the present Office Action, the Office opined, with the claimed invention as a road map, that "[w]hen Inaba was combined with Kobayashi[,] an inductor was motivated to be placed on the anode side connection to ground. This combination formed a parallel connection on the anode side between the resistor of Inaba and the newly added inductor on the ground connection line. The original combination with Kobayashi thus formed the anode side parallel connection while the combination with Nagarajan formed the cathode side connection" (see paragraph spanning pages 2 and 3 of the Office Action). Accordingly, even though the Office previously rejected claim 4 on the basis of Nagarajan to propose an arrangement of a resistor connected in parallel with an inductance element to the anode of an optical semiconductor element, the Office modified its interpretation of the applied references. The Office now alleges that the inductor L9 and resistor R of Kobayashi correspond to the arrangement of the second bias circuit of claim 1 (i.e., a resistor connected in parallel with an inductance element to the anode of the optical semiconductor element), and that the resistor connected in parallel with the inductor in the DC bias circuit 16 of Nagarajan correspond to the first bias circuit of claim 1 (i.e., a resistor connected in parallel with an inductance element to the cathode of the optical semiconductor element.

According to the "Response to Arguments" on pages 2 to 3 of the Office Action, the combination of Inaba and Kobayashi is alleged to form the anode side parallel connection (allegedly corresponding to the second bias circuit, as recited in claim 1), while the combination of Inaba and Nagarajan forms the cathode side parallel connection (allegedly corresponding to the first bias circuit, as recited in claim 1).

Applicants respectfully disagree with this interpretation. As described, for example, in line 19 on page 9 to line 2 on page 10 of the specification, in an optical semiconductor device of the claimed invention, a "first bias circuit" and a "second bias circuit" are provided in order to prevent a resonance caused by reactance components of the inductance elements, inductances of wire bonds, capacities of pads, and parasitic capacitances of the inductance elements, and cut off electric signals at high frequencies in wide frequency bands. For instance, as described in line 19 on

page 4 to line 5 on page 6 of the specification, the resonance causes great deterioration of the optical output waveform of the optical semiconductor device. Thus, the "first bias circuit" and the "second bias circuit" are provided in the optical semiconductor device to prevent such resonance. Accordingly, the arrangement of the constituent elements of the optical semiconductor device as recited in claim 1, for example, improves the deterioration of an optical output waveform, and improves the quality of the optical output waveform. These features and effects are not achieved by the proposed combination of references.

For example, as described in lines 2-8 on page 20 of the specification, in the optical semiconductor device of the claimed invention, a first inductance element (e.g., solenoid 21a in Fig. 1) having a high impedance with respect to a high frequency and a first resistor (e.g., resistor 22a in Fig. 1) connected in parallel to the first inductance element (e.g., solenoid 21a) and reducing a Q value for preventing a resonance constitute a "first bias circuit 28a" (first bias circuit as recited in claim 1), while a second inductance element (e.g., solenoid 21b in Fig. 1) having a high impedance with respect to the high frequency and a second resistor (e.g., resistor 22b in Fig. 1) connected in parallel to the second inductance element (e.g., solenoid 21 b) and reducing the Q value for preventing the resonance constitute a "second bias circuit 28b" (second bias circuit as recited in claim 1). In other words, the above constitution of the "first bias circuit" and the "second bias circuit" including a combination of the inductance element having a high impedance with respect to a high frequency and a "resistor" connected in parallel to the inductance element and reducing the Q value for preventing the resonance is a unique feature of the claimed invention to attain the above-described features of the claimed invention.

Additionally, in the optical semiconductor device of the claimed invention, as recited in independent claims 1 and 14-17, a "first conductor line" and a "first inductance element" are connected to the cathode of the optical semiconductor element, while a "second conductor line" and a "second inductance element" are connected to the anode of the optical semiconductor element, and the "first conductor line" and the "second conductor line" constitute a pair of differential lines. For example, as disclosed in line 20 at page 27 to line 4 at page 28 of the specification, since the "bias circuits" (each of them includes an inductance element and a resistor)

are arranged on both sides of the optical semiconductor element to which the differential lines are connected, if the optical semiconductor element is assumed as the equivalent circuit, the two bias circuits appear to be connected in series to the optical semiconductor element. Hence, the amplitude of the resonance can be reduced, the sharp decline (ripple) of the passing characteristics followed by the arrangement of the "bias circuits" can be improved, the quality of the optical output waveform can be improved, and good transmission characteristics can be thereby obtained. Accordingly, the optical semiconductor device of the claimed invention improves the deterioration of an optical output waveform, and improves the quality of the optical output waveform.

On the other hand, the purpose of Inaba is to provide a "laser drive circuit" capable of precisely controlling a laser beam intensity. In order to attain this object, as disclosed in the Abstract, for example, first, the "laser drive circuit" modulates a laser beam intensity emitted from a laser device to a maximum power and a minimum power in accordance with first and second values of a binary signal. Second, the "laser drive circuit" produces a "maximum error detection signal" representing a difference between the detection output signal applied thereto and a maximum reference and a "minimum error detection signal" representing a difference between the detection output signal applied thereto and a minimum reference. Third, the "laser drive circuit" samples and holds the "maximum error detection signal" and the "minimum error detection signal". Finally, the "laser drive circuit" controls the maximum power and the minimum power of the laser beam emitted from the laser device in accordance with the "maximum error detection signal" and the "minimum error detection signal". Accordingly, the purpose and function of the "laser drive circuit" disclosed in Inaba is merely to control a laser beam intensity. Therefore, Inaba does not disclose, suggest or contemplate the features and effects of the optical semiconductor device of the claimed invention in improving the deterioration of an optical output waveform.

The purpose of Kobayashi is to provide an "electronically cooled semiconductor laser module" capable of preventing the lowering of optical frequency response level in bands employed for public communications. In order to attain this object, Kobayashi discloses that by changing the inductance of the ground line

between module package and chip-mounted carrier of the semiconductor laser module, the resonance frequency of a resonance circuit made up by including the ground line is shifted so as to deviate from the frequency band of public communications used by a modulation signal transmitting device. Accordingly, the purpose and function of the "electronically cooled semiconductor laser module" disclosed in Kobayashi is merely to prevent the lowering of optical frequency response level. Therefore, Kobayashi does not disclose, suggest or contemplate the features and effects of the optical semiconductor device of the claimed invention in improving the deterioration of an optical output waveform.

The purpose of Nagarajan is to provide an "optical transmission link" having both a transmitter module and a receiver module operable under uncooled conditions without the need of costly cooling equipment such as thermoelectric coolers. In order to attain this object, the "optical transmission link" includes both a semiconductor laser diode source and an optical receiver module that are both designed to operate uncooled under high frequencies over a wide temperature range without significant changes in signal bandwidth and at temperatures in excess of 125 Celsius. Accordingly, the purpose of the "optical transmission link" disclosed in Nagarajan is merely to provide the "optical transmission link" having both a transmitter module and a receiver module operable under uncooled conditions. Therefore, Nagarajan does not disclose, suggest or contemplate the features and effects of the optical semiconductor device of the claimed invention in improving the deterioration of an optical output waveform.

Accordingly, based on the disclosures of Inaba, Kobayashi and Nagarajan, one skilled in the art would not have reason or been motivated to arrive at the features of the claimed invention. In particular, one skilled in the art would not have reason or been motivated to achieve the unique circuit configuration of the claimed invention in which two bias circuits (each of them including an inductance element and a resistor) are arranged on the both sides of the optical semiconductor element to which the differential lines are connected. Accordingly, one skilled in the art would not have been motivated to provide parallel resistor and inductor combinations to both the anode and cathode of the laser diode LD1 of Inaba. The Office's proposed modification of Inaba would not be sensible to one skilled in the art

based on the respective disclosures of Inaba, Kobayashi and Nagarajan.

For at least the foregoing reasons, Applicants respectfully submit that the applied references do not disclose, suggest or contemplate the recited arrangement of the recited combination of the optical semiconductor element, first and second conductor lines, first and first and second inductance elements, and first and second bias circuits, as recited in claim 1, as well as their corresponding features in claims 14-17. Applicants respectfully submit that the Office's purported combination of Inaba, Kobayashi and Nagarajan is derived from Applicants' claimed invention, and would not be sensible to one skilled in the art based on the respective disclosures of the applied references.

Applicants respectfully submit that one skilled in the art would not have reason or been motivated to combine Inaba, Kobayashi and Nagarajan in the manner proposed by the Office to arrive at the recited arrangement of the recited combination of the optical semiconductor element, first and second conductor lines, first and first and second inductance elements, and first and second bias circuits, as recited in claim 1.

Therefore, Applicants respectfully submit that claim 1 is patentable over Inaba, Kobayashi and Nagarajan, since Inaba, Kobayashi and Nagarajan, either individually or in combination, do not disclose or suggest all the recited features of claim 1.

In addition, Applicants respectfully submit that claims 14-17, which recite a second bias circuit similar to the second bias circuit of claim 1, are also patentable over Inaba, Kobayashi and Nagarajan, for similar reasons to those presented above with respect to claim 1.

Therefore, Applicants respectfully request that claims 1 and 14-17 are patentable over Inaba, Kobayashi and Nagarajan, since one skilled in the art would not have reason or been motivated to combine the references in the manner proposed by the Office.

B. Dependent claims 2, 5, 19 and 20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Inaba and Kobayashi in view of Nagahori, Takeshi et al. ("An Analog Front-End Chip Set Employing an Electro-Optical Mixed Design on SPICE for 5-Gb/s/ch Parallel Optical Interconnection." IEEE Journal of Solid-State Circuits, Volume 36, No. 12, pp 1984-1994, December 2001, hereinafter "Takeshi"). Dependent claim 6 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Inaba, Kobayashi, Takeshi and further in view of Ito et al. (U.S. Patent No. 4,975,664, hereinafter "Ito").

In addition, dependent claims 7-9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Inaba, Kobayashi, Takeshi, Ito and further in view of Kobayashi et al. (U.S. Patent No. 5,982,793, hereinafter "Kobayashi '793"). Lastly, dependent claims 10-11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Inaba, Kobayashi and further in view of Kobayashi '793.

As discussed above, Inaba, Kobayashi and Nagarajan, either individually or in combination, do not disclose or suggest the recited combination of the optical semiconductor element, first and second conductor lines, first and first and second inductance elements, and first and second bias circuits, as recited in claim 1, as well as their corresponding features in claims 14-17.

Similarly, Takeshi, Ito and Kobayashi '793 also each fail to disclose or suggest the recited combination of the optical semiconductor element, first and second conductor lines, first and first and second inductance elements, and first and second bias circuits, as recited in claim 1, as well as their corresponding features in claims 14-17.

Consequently, Takeshi, Ito and Kobayashi '793 cannot cure the deficiencies of Inaba and Kobayashi for failing to disclose or suggest all the recited features of claims 1 and 14-17.

Accordingly, no obvious combination of Inaba, Kobayashi, Nagarajan, Takeshi, Ito, and Kobayashi '793 can result in the subject matter of claims 1 and 14-17, since these references, either individually or in combination, fail to disclose or suggest all the recited features of claims 1 and 14-17.

Therefore, Applicants respectfully submit that claims 1 and 14-17, as well as claims 2-13 and 18-22 which depend therefrom, are patentable over the applied references.

Dependent claims 2, 5 and 18-22 recite further distinguishing features over the applied references, and are also patentable by virtue of depending form claims 1 and 14-17. The foregoing explanation of the patentability of independent claims 1 and 14-17 is sufficiently clear such that it is believed to be unnecessary to separately demonstrate the additional patentable features of the dependent claims at this time. However, Applicants reserve the right to do should it become appropriate.

II. Conclusion

In view of the foregoing remarks, it is respectfully submitted that the present application is clearly in condition for allowance. Accordingly, favorable examination and consideration of the instant application are respectfully requested.

If, after reviewing this response, the Examiner believes there are any issues remaining which must be resolved before the application can be passed to issue, the Examiner is respectfully requested to contact the undersigned by telephone in order to resolve such issues.

Respectfully submitted,

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